

Interpretation of lock-in thermography on thin film solar cells considering dissipative and Peltier contributions

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Abstract

We describe the measurement and modeling of lock-in thermograms of crystalline silicon on glass (CSG) thin film silicon solar modules for a range of bias voltages. For that purpose, a voltage series of lock-in thermograms for a single cell in the module is measured and compared to the area heat production distribution resulting from a Spice electronics simulation. The point spread function for the highly heat conductive layer on a thick glass substrate as well as Peltier effects at p⁺ and n⁺ contact holes are taken into account. This makes it possible to extract relevant cell performance parameters like the area diode saturation current and nonlinear edge shunting current densities.

1. Theory and simulation overview

1.1 Sample description and module layout

The sample analyzed here was produced at the experimental production site of CSG Solar in Thalheim, Germany. It consists of a 3 mm glass substrate with a texture made from deposited glass beads for light-trapping, anti-reflection coating, the p⁺-p-n⁺ silicon diode and back side contacting.

CSG employs an unusual interdigitated contacting scheme [1], which consists of 0.5 mm wide Al pads spanning 2 cells each. Each contact pad has 30 contact holes, half of them contact the n⁺ layer of one cell and the other 15 contact the p⁺ layer of the next cell. The whole back surface of the cell is covered by these Al pads resulting in a low series resistance of the module but suppressing shunting effects due to its high resistance parallel to the cell axis [1,2].

1.2 Influence of Peltier effects

In contrast to standard wafer-based solar cells and many other thin film concepts, in the CSG contacting scheme p⁺ and n⁺ contacts are beside each other in the image plane and thermoelectric effects become visible. When a forward current is driven through the module, the metal-p⁺ contact (positive Peltier coefficient of p⁺ silicon, metal Peltier coefficient negligible) and the n⁺-metal (negative Peltier coefficient of n⁺ silicon) contact both show pronounced cooling effects for typical biases of 300 to 500 mV/cell.

Thermoelectric effects are of no consequence to the performance of the solar module and the energy taken from the environment at the contact holes needs to be dissipated at some place in the module. Roughly speaking, this happens during the recombination process, thus possibly several millimeters distant from the cooling effect at the contact hole. The corresponding terms are (q^P : heating/cooling power density, j : current density, Π : Peltier coefficient)

$$\text{Al to p}^+ : q^P = (-j) \times \Pi_{p^+},$$

$$\text{n}^+ \text{ to Al} : q^P = j \times \Pi_{n^+},$$

$$\text{p}^+ \text{ to n}^+ : q^P = j \times (\Pi_{p^+} - \Pi_{n^+}).$$

In consequence, the image of local heat dissipation as recorded using dark lock-in thermography (DLIT) at forward bias is a superposition of thermoelectric heat redistribution and actual power dissipation. There is no straightforward way to separate both effects. Therefore, we chose to do an *electro-thermal reverse simulation* of the thermograms to extract the cell parameters.

1.3 Point spread function

The thermal part of our electro-thermal simulation deals with the question: What is the thermal wave pattern caused by a given distribution of heat sources (W/m²)? This is found by calculating the thermal point spread function (PSF) for a point-like heat source and convoluting it with the simulated heat source pattern.

In LIT it is generally assumed, as a first approximation, that every sample of interest is either thermally thin or

thermally thick. Solutions for the PSF of both cases can be readily taken from literature [3,4,5]. The geometry of 1.5 μm silicon on 3 mm glass at available lock-in frequencies of roughly 1 to 50 Hz, however, is poorly described by either approximation. Therefore, an analytical expression for the point spread function was developed and applied:

$$P(r) = \frac{1}{2\pi} \int_0^{\infty} \frac{J_0(rk)kdk}{d\lambda_f(i\omega/D_f + k^2) + \lambda\sqrt{i\omega/D + k^2}},$$

where ω is the lock-in frequency ($2\pi f$), d is the layer thickness, λ the thermal conductivity, D the thermal diffusivity and J_0 denotes the Bessel function of the second kind of zero order. Index f refers to properties of the thin layer. Figure 1 shows this result for a thermally thin layer of 1.5 μm silicon on a thick glass substrate along with the results for a thermally thin silicon layer (of thickness 200 μm) and a thermally thick glass substrate alone. Derivation, interpretation and experimental verification of this result will be presented in an upcoming publication [6].

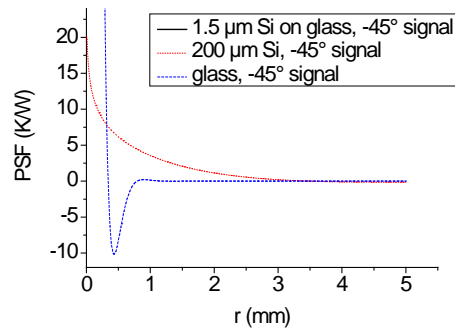


Fig. 1. Point spread functions for the case of silicon on glass in comparison with the limiting cases of heat wave propagation through thermally thin and thick media (10 Hz lock-in frequency, -45°). The -45° signal is the one with maximum intensity for the cases of thermally thick glass and the thin layer on glass. The behavior of silicon on glass is clearly in between the extreme cases and poorly described by both.

A further complication appears at the cell edges because the individual solar cells are separated by a laser groove. Cutting the silicon on the glass interrupts the highly heat conductive layer and thus has an impact on the heat conduction. This problem of heat conduction close to the cell edges is especially important when investigating nonlinear groove shunting and was modeled using the finite element (FEM) package COMSOL. The results for the -45° signal (which is used in the experiments) are shown in figure 2. The simulated system response to a line-shaped heat source (line spread function, LSF) at the groove edge shows a strong signal drop due to the groove for the 25 μm groove width in the samples (even for a simulated 1 μm groove, this drop is still prominent). Comparison with the LSF for a system with no groove suggests the interpretation, that heat being conducted in the thin silicon layer is reflected at the groove while the heat being conducted through the glass passes undisturbed.

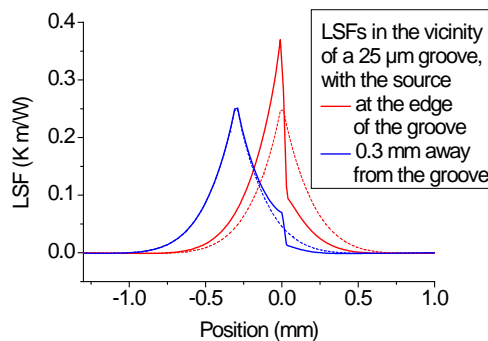


Fig. 2. Thermal response to a line-shaped heat source (-45° signal) at the groove edge and 0.3 mm away from it. Part of the heat is directly reflected into the silicon. This reflection effect happens (less strongly) for increased distance to the groove until it gets small for distances bigger than 0.3 mm. The dashed curves show the undisturbed LSFs.

Two conclusions can be drawn from figure 2. Firstly, the fact that the highly heat conductive silicon layer on the

sample is cut strongly influences the shape of the temperature response. Secondly, the integral under the curves does not depend on the distance between source and groove. This is plausible because the ratio of heat being conducted in the glass and in the silicon is not affected by the groove, which is easily confirmed in the simulation.

Therefore, although the grooves do have a strong influence for distances from source to groove below 0.3 mm, the analytical PSF (for “infinite” distance to the groove) can still be used close to the grooves as long as the heat reflections seen in figure 2 are taken into account and only the *integral* of the signal is evaluated over the characteristic length scale.

1.4 Electrical (Spice) model

Electrically, each cell in the module consists of an area diode of 6 mm width and approximately 1 m length with a low sheet resistivity ($< 500 \Omega^{\text{sq}}$) top and bottom layer. The material is somewhat damaged close to the grooves that separate the individual cells. This can be modeled by assuming an additional, line-shaped diode on both sides of each cell. A straightforward discrete equivalent circuit for this model is found by putting nodes at the locations of contact holes, both in the n^+ and the p^+ layer, and at the cell edges. These are then connected with the corresponding elementary diodes and sheet resistances. Because in the real samples, there is a certain spacing between the outermost contact holes and the cell edge, an additional elementary diode with no corresponding contact hole was introduced. This layout is shown in figure 3.

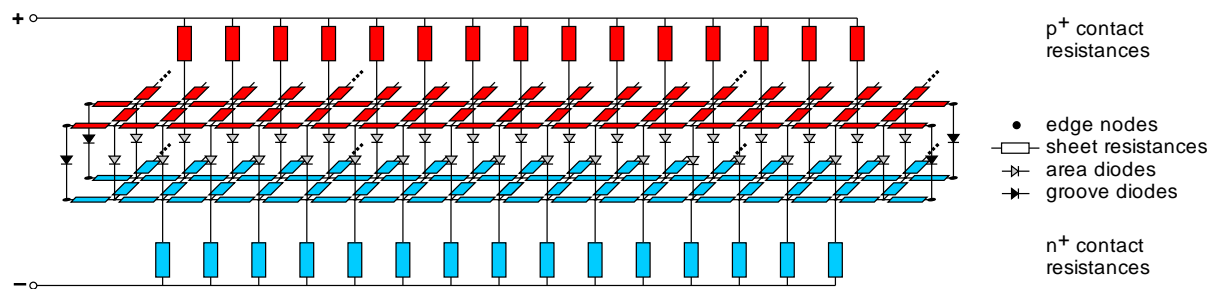


Fig. 3. Spice model for a CSG cell. In the front line of diodes, the n^+ region (blue) is connected to the next cell of the module by 15 contact holes (below). In the second line, 15 contact holes (above) contact the p^+ region (red) to the previous cell. The elementary diodes, distributed according to the location of the contact holes, are interconnected by the sheet resistivity in the p^+ and n^+ layers.

Using the measurements described in section 2.2, the values of the resistors can be directly calculated from the geometry of the sample. This leaves the most interesting parameters open, which are the dark saturation currents in the area and at the grooves, respectively. In crystalline cells it is generally assumed that the diode current in any undamaged part of the cell (far from the edge, no scratches) has an ideality factor of 1. This assumption is too optimistic for the central part of the cell, probably due to the fact that the average crystallite diameter is only approximately $2 \mu\text{m}$. Also the ideality factor of the groove diodes is unknown. Since measurements were only done in the range of 300 to 500 mV, it is admissible to describe the diode behavior in this range by a simple one-diode model with an effective ideality factor n to be determined from the measurements, $I = A_j_0 [\exp(V/nkT) - 1]$.

1.5 Simulation procedure

The reverse simulation is an iterative process. Starting off with the measured values for the resistances, the measured Peltier coefficients and diode current values derived from the overall $I-V$ characteristic, the electrical simulation gives a power and current distribution pattern. This pattern is then convoluted with the thermal point spread function giving a simulated LIT image. The parameters of the electrical model are then adjusted until the agreement between experiment and simulation is satisfactory.

2. Experimental

2.1 Measurement of the Peltier coefficient

In a recent contribution we described how to measure the Peltier coefficient of semiconductor material thermographically using DLIT [7]. The procedure is slightly modified for a resistance test structure that is convenient for the module manufacturer. The basic idea is to exploit that in a purely resistive structure, a bias polarity change causes a change of sign for Peltier heat redistribution whereas Joule heat dissipation remains unchanged. This is true for any distribution of

resistivity as long as it remains fully ohmic. Adding and subtracting lock-in thermograms for positive and negative bias (S^+ and S^-) thus gives images of Joule heat dissipation and Peltier type transport:

$$S^J = (S^+ + S^-)/2,$$

$$S^P = (S^+ - S^-)/2.$$

Resistivity test structures made by the cell manufacturer replace the normal pattern of p^+ and n^+ contact holes by a pattern where *all* contact holes in one structure are either p^+ or n^+ . The resulting structure is then fully described by sheet resistivities and contact hole resistances alone. Figure 4 shows the thermograms obtained for these test structures that lead to a Peltier coefficient Π of $+(90 \pm 5)$ mV for the p^+ region and $-(90 \pm 5)$ mV for the n^+ region.

The physical meaning and origin of these values is detailed in [7]. Following the procedures outlined there, reasonable doping concentration values in the order of 10^{19} cm^{-3} as specified for this type of solar module are obtained. It is also found that for doping concentrations in the order of 10^{19} cm^{-3} the Peltier coefficient depends only weakly on the doping concentration such that these values should be applicable for all CSG samples. Further details on the application of this method [7] to CSG resistivity test structures can be found in [8].

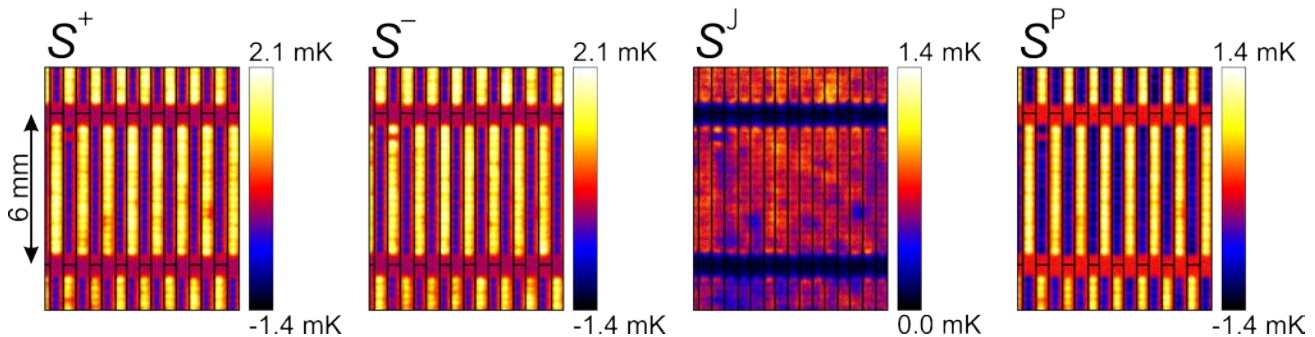


Fig. 4. Measured signals S^+ , S^- for positive and negative bias and corresponding Joule S^J and Peltier S^P contributions calculated by adding and subtracting the measured signals.

2.2 Measurement of electrical contact and sheet resistance

In the simulation there are many parameters to fit to the measured data: area j_0 and n , j_0 and n for both grooves, sheet resistances for p^+ and n^+ as well as contact hole resistances for p^+ and n^+ contacts. It is therefore desirable to reduce the number of parameters or, at least, to get some good starting values for them.

The contact and sheet resistances for the CSG structure can be measured directly. For that, the interconnection needs to be cut. The sheet resistance in both p^+ and n^+ as well as the resistance of the p^+ and n^+ contact holes can be measured conveniently using two different arrangements of spring-loaded contact pins. The contact pins are placed on Al pads with contact holes of the same type (see figure 5). For the geometry of the samples, the measured value for the contact resistance is that of all 15 contact holes per pad and cell in parallel. The measured sheet resistance is that of a current flowing homogeneously through a length of 1 mm (two pads) in a 6 mm wide (cell width) conductor.

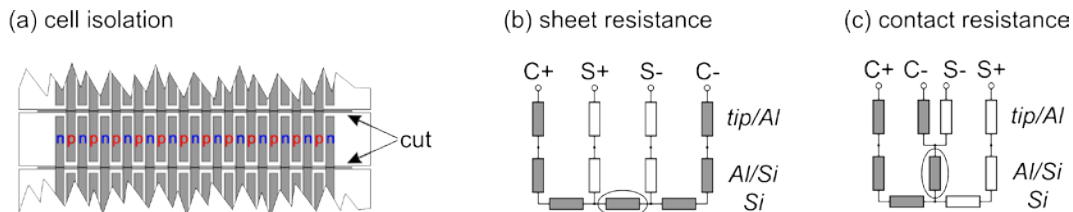


Fig. 5. For meaningful p^+ and n^+ layer resistance measurements, the interconnections need to be cut as shown in (a). Then, the sheet resistance spanning two contact pads can be measured as shown in (b) and the contact resistance of the contact holes is found independently using the arrangement shown in (c). Shaded resistors are those subject to a potential drop due to the current from C^+ to C^- . The circled resistor is measured.

To get statistically sufficient data, a small contact pin holder was constructed for an x-y-z stage. Table 1 shows the averaged resistance values. Note that the standard deviation does not reflect the measurement error but the variation in the measured data.

Table 1. Contact and sheet resistances for the sample. The contact resistance values correspond to the 15 contact holes in parallel (the contact hole resistance thus being approximately 60 Ω .) The sheet resistance values were measured for a 6 mm wide, 1 mm long path (the sheet resistance thus being approximately 500 Ω^{sq}).

	p (Ω)	n (Ω)
contact resistance	3.7 ± 0.3	4.5 ± 0.3
sheet resistance	92.8 ± 1.4	74.2 ± 1.2

2.3 Single cell contact preparation

The edges of the individual cells are separated by 25 μm thick grooves, which is below the resolution of LIT for experimentally available lock-in frequencies (see figure 1). Therefore, signals from the edge of one cell cannot be safely distinguished from signals from the edge of the neighboring cell. To avoid this difficulty, a single cell was contacted. This was done by evaporating 50 nm gold layers which short the neighboring cells (see the contacting scheme shown in figure 7a). Contact resistance to the conductive adhesive used seems to be a problem which is why a 4-point contacting scheme as shown in figure 7b was adopted.

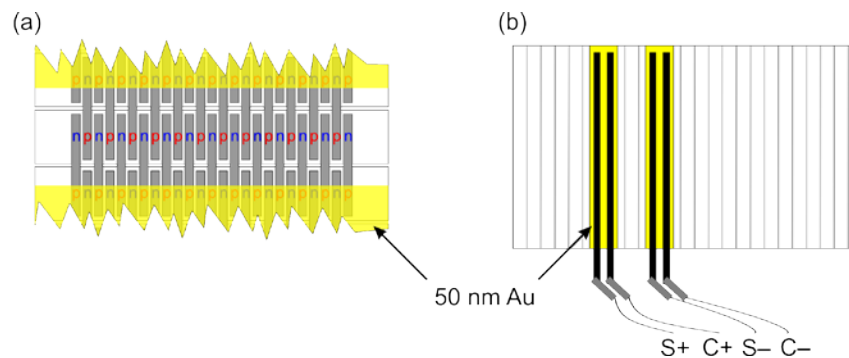


Fig. 7. 4-point contacting scheme for a single cell in a CSG module.

2.4 DLIT measurement: voltage series

For sufficient DLIT signal resolution and phase, the camera faced the active layer of the cell and not the glass side which is opaque for thermal radiation. Since it is covered with the (high reflectivity) aluminum of the contacting scheme, a black PE foil was sucked to the sample to achieve sufficient IR emission. Temperature calibration was done using a temperature-controlled chuck. Since the thermal contact resistance between the chuck and the rigid glass of the module is very high, the temperature on the surface was measured using a (calibrated) pyrometer. Calibrating the camera in this way has the additional benefit that it evens out emissivity gradients in the foil.

To find the experimental proportionality factor between power input and temperature response, the sample cell was fully ($100 \times 6 \text{ mm}^2$) imaged at 0.5 V, 17 mA/cm^2 . The integral of the image related to the overall power consumption gives a proportionality factor of 0.026 $\text{mK m}^2/\text{W}$. This factor does not depend on magnification and was applied to close-up images of approximately $10 \times 10 \text{ mm}^2$. DLIT was performed at voltages ranging from 300 to 500 mV in steps of 50 mV. At 300 mV, an integration time of 2 h was necessary to achieve a good signal-to-noise ratio, which makes voltages < 300 mV experimentally unavailable. On the other hand, voltages over 500 mV are not meaningful as they quickly exceed the short circuit current of the illuminated cell of approximately 25 mA/cm^2 . Due to the module design, series resistance effects become overwhelmingly important at this point and a more detailed cell model would be necessary.

3. Fit results and discussion

Iteratively fitting the simulated to the experimental images gives the following values for the diode currents. Changing the dark current values about $\pm 10\%$, causes the experimental and simulated data to diverge appreciably, this is

thus a measure of the uncertainty. The ideality factors are also somewhat arbitrary (± 0.2), provided the j_0 are altered accordingly.

Table 2. Diode properties found manually fitting lock-in thermograms to simulated data. Coincidentally, $j_{0,groove}$ was almost evenly distributed between both cell edges for this sample (51 % for the left groove).

$j_{0,area}$ (A/cm ²)	n_{area}	groove ratio	$j_{0,groove}$ (A/cm ²)	n_{groove}
4.0×10^{-7}	1.7	51 %	4.5×10^{-6}	2.5

With these values, the following images for experimental and simulated data are obtained.

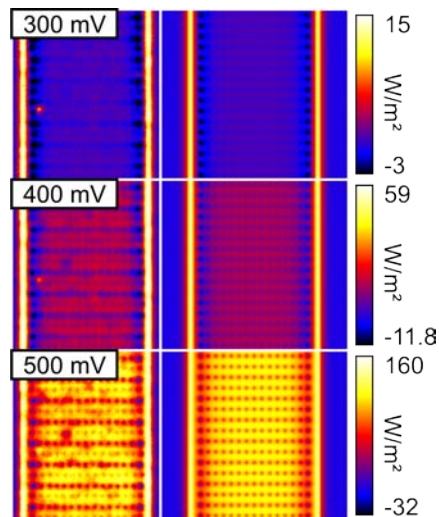


Fig. 8. Maps of heating power density from experiment (left) and simulation (right) at low, medium and high voltages. The relative intensity of the groove signal diminishes at higher voltages, while that of the area current increases. This suggests a higher ideality factor at the grooves.

A certain dissimilarity between experimental and simulated data is present in the contact holes. In the experiment, every second line of contacts is much less intensely seen than in the simulated data. This cannot be explained by series resistance effects. Our hypothesis is that the emissivity foil does not completely cover the bottom of the contact holes (140 μm wide, shallow p^+ holes $\approx 3 \mu\text{m}$, deeper n^+ holes $\approx 4 \mu\text{m}$), but does more so in the shallow contact holes. Estimations show that a 4 μm air gap causes an intensity loss of approximately 15 % at 10 Hz, which might explain the discrepancies seen in our experiments. Avoiding these air gaps would be preferable, though, which might be accomplished if a suitable removable black paint was found.

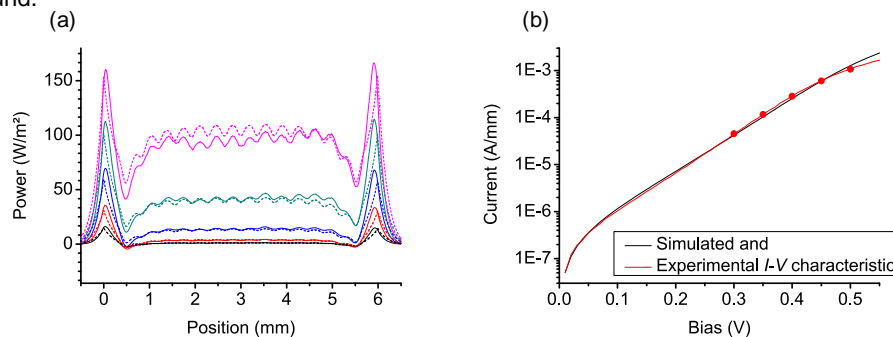


Fig. 9. (a) Vertically averaging line-scans from 300 mV (black) to 500 mV (magenta) in steps of 50 mV for experimental (full lines) and simulated data (dashed lines). (b) Comparison of current per mm cell width. The voltages at which the LIT images of the cell portion used in the fitting procedure were taken are indicated by dots.

The actual fitting can be done much more easily using horizontal line-scans (averaging the data along the cell axis). Figure 9a shows experimental and simulated data. These show satisfactory agreement, even in details such as the exact shape of the depressions of the Peltier cooling close to the cell edges and the amplitude of the central signal variation due to the inner contact holes. The heat reflection at the groove edge back to the cell interior for the heat conducted in the silicon layer is seen as a marked asymmetry of the experimental groove peaks (see section 1.3). The simulated curves do not show this asymmetry as they were calculated neglecting the influence of the grooves.

Figure 9b compares the (normalized) I - V characteristic of the entire sample ($100 \times 6 \text{ mm}^2$) with that in the simulated structure ($8 \times 6 \text{ mm}^2$). In the analyzed range from 300 mV to 500 mV the agreement is good. As the parameters of the simulated structure were determined from the LIT images of only a small portion of the real structure, a certain amount of deviation is normal. Below 300 mV, the agreement is still surprisingly good, although this range was not considered in the fit process.

4. Conclusions

We have shown a quantitative analysis for CSG thin film solar modules. The quantitative evaluation of the lock-in thermograms on these thin film solar cells poses new challenges compared to the more established application of DLIT to standard cells. These are: Peltier heat redistribution from the contact holes to shunts and bad cell regions and a more complicated heat conduction regime which is neither thermally thin nor thick.

We have shown how these difficulties can be overcome using an iterative approach. The good agreement between simulation and experiment shows that with the aid of local network simulations the thermal response of thin film solar cells in DLIT is now well understood.

The main drawback of our approach is its complexity. We are hoping to develop suitable simplified models whose applicability can be checked by using the formalism presented here.

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